REMARKS

Claims 1 – 19 are currently pending in the application. The above amendment does not add new matter to the application and is fully supported by the specification. Additionally, Applicants submit that the amendments to the claims have been made to rectify claim objections, and not to overcome any applied prior art. Reconsideration of the rejected claims in view of the above amendments and the following remarks is respectfully requested.

Information Disclosure Statements

Applicants note with appreciation the Examiner's indication that the Information Disclosure Statements filed August 4, 2004 and August 9, 2004 have been considered.

Objection to the Drawings

The drawings were objected to for failing to comply with 37 C.F.R. 1.84(p)(4) and for failing to comply with 37 C.F.R. 1.84(g). Applicants have submitted herewith amended drawings, incorporating the Examiner's suggested change and with increased margins.

Accordingly, Applicants respectfully request that the objection to the drawings be withdrawn.

Claim Objections

Claims 2, 3, 12 and 18 have been objected to by the Examiner. Claims 2, 3, 12 and 18 have been amended to reflect the Examiner's suggestions.

However, the Examiner objected to claim 3 for not having an "or" and claim 18 for using an "and" rather than an "or". Applicants have amended claim 3 to include an "and". Applicants respectfully submit that "and" in the context of "at least on of" language is proper.

Accordingly, Applicants respectfully request that the Examiner withdraw the objections to claims 2, 3, 12 and 18.

35 U.S.C. § 102 Rejection

Claims 1 – 11 were rejected under 35 U.S.C. § 102(e) for being anticipated by U.S. Patent 6,092,225 issued to Gruodis et al. (hereinafter Groudis). Claims 12 – 18 were rejected under 35 U.S.C. § 102(e) for being anticipated by U.S. Patent 5,872,797 issued to Theodoseau (hereinafter Theodoseau). These rejections are respectfully traversed.

Initially, Applicants respectfully note that claim 19 was not rejected on the merits. While Applicants acknowledge that claim 19 was grouped with claim 1 in the body of the rejection, claim 19 was not stated as being rejected. Accordingly, Applicants submit that the next Office Action cannot be final, as all the claims were not treated on the merits and all issues were not clarified. See MPEP § 706.

To anticipate a claim, each and every element set forth in the claim must be found, either expressly or inherently described, in a single prior art reference. MPEP §

2131. Applicants submit that neither Groudis nor Theodoseau disclose each and every feature of the claimed invention.

Rejection of Independent Claim 1 over Groudis

The present invention generally relates to a method and system for testing an electronic circuit. More specifically, claim 1 recites, in pertinent part:

> defining a first initial vector;
> defining at least one segment within the first initial vector;
> offsetting the first initial vector a predetermined amount within the at least one segment;
> defining a counter loop comprising loops of the first initial vector within the at least one segment to produce a first set of vectors in accordance with the counter loop;
> defining a progressively changing variation of the first initial vector for each loop of the counter loop so at least one vector of the first set of vectors varies from the first initial vector;
> and coupling the at least one segment having the first set of vectors including the varied at least one vector to produce a final pattern for a circuit under test.

The Examiner asserts that Groudis discloses these features in column 3, lines 49 – 62, column 4, line 10 to column 6, line 51, and column 11, lines 20 – 45. Applicants respectfully disagree.

The Examiner asserts that Groudis discloses defining at least one segment within the first initial vector. While Applicants acknowledge that Groudis discloses "segments", Applicants submit that the segments disclosed in Groudis are segments of the test cycle, and not segments within the first initial vector, as recited in claim 1. More specifically, Groudis discloses an integrated circuit tester that organizes an IC test into a succession of test cycles, each test cycle being divided into four segments. The tester includes a separate tester channel for carrying out a test activity at each IC pin during

each segment of the test cycle. The tester also includes a separate pattern generator for each channel. Each pattern generator concurrently generates four vectors at the start of each test cycle. Each vector tells the channel what activity it is to carry out during a separate segment of the test cycle. Each pattern generator includes a low-speed vector memory storing large blocks of vectors at each address and a cache memory system for caching blocks of vectors read out of the vector memory. A vector alignment circuit selects from among the cache memory output vectors to provide the four vectors to the channel for the four segments of the test cycle. Therefore, Groudis does not contain each and every element of the claim, and does not anticipate the claimed invention.

Additionally, the Examiner asserts that the vector alignment circuit 30 of Groudis discloses offsetting the first initial vector a predetermined amount within the at least one segment, as recited in claim 1. Applicants submit, however, that the vector alignment circuit does not offset the first initial vector a predetermined amount within the at least one segment. Applicants acknowledge that Groudis discloses the vector alignment circuit including a register for delaying the sixteen output vectors of the cache memory system by one test cycle and applying them as inputs to the routing switch. However, Applicants submit that this is not offsetting the first initial vector a predetermined amount within the one segment. Rather, Groudis expressly discloses that the vector alignment circuit selects from among the cache memory output vectors to provide the four vectors to the channel for the test cycle. In other words, the vector alignment circuit of Groudis, selects four vectors from a memory storage of many vectors, and those selected four vectors are used in the four segments of the test cycle. Therefore, Groudis does not

contain each and every element of the claim, and does not anticipate the claimed invention.

Rejection of Dependent Claims 2 – 11 over Groudis

Applicants respectfully submit that claims 2 – 11 depend from a distinguishable independent claim, and are allowable based upon the allowability of the independent claim.

Additionally, Applicants submit that Groudis does not disclose defining a data control vector to allow a prescribed input format of the first initial vector, as recited in claim 8. Applicants note that the Examiner has not specifically identified what is asserted to be the data control vector in Groudis. Applicants respectfully request that, if the Examiner maintains this rejection, that the Examiner specifically identify what is asserted to be the data control vector to allow a prescribed input format of the first initial vector.

Furthermore, Applicants submit that Groudis does not disclose defining a new format vector to be added to the first initial vector to reconfigure the shape of the first vector, as recited in claim 9. Applicants note that the Examiner has not specifically identified what is asserted to be the new format vector in Groudis. Applicants respectfully request that, if the Examiner maintains this rejection, that the Examiner specifically identify what is asserted to be the new format vector to be added to the first initial vector to reconfigure the shape of the first vector.

Moreover, Applicants submit that Groudis does not disclose defining a second vector; allocating a second segment configured to contain the second vector; and offsetting the second vector a predetermined amount within the second segment, as

recited in claim 10. As discussed with regards to claim 1, Applicants submit that the "segments" disclosed by Groudis are segments of a test cycle. Therefore, Groudis does not contain each and every element of the claim, and does not anticipate the claimed invention.

Accordingly, Applicants respectfully request that the rejection over claims 1 – 11 be withdrawn.

Rejection of Independent Claim 12 over Theodoseau

The present invention generally relates to a method and system for testing an electronic circuit. More specifically, claim 12 recites, in pertinent part:

> selecting a macro definition file defining at least one vector;
> forming a control bit definition file configured to be added to the at least one vector;
> creating a pattern definition file configured to selectively alter a portion of the at least one vector;
> creating a global definition file configured to alter the entire vector; and
> combining the macro, control bit, pattern formats, and global definition files to form a final vector to produce a final pattern.

The Examiner asserts that Theodoseau discloses these features in column 6, line 36 to column 9, line 50. Applicants respectfully disagree.

The Examiner asserts that the counter control 402 of Theodoseau discloses forming a control bit definition file configured to be added to the at least one vector, as recited in claim 12. Applicants submit, however, that Theodoseau does not disclose the counter control forming a control bit definition file and does not disclose the counter control configured to be added to the at least one vector.

Theodoseau discloses a user-specified nested sequence of counters, logical combination of the counter outputs and generation of corresponding vectors for application to exercise integrated circuit devices. More specifically, Theodoseau

discloses a counter control 402 controls the organization of the vectors, or sequences of vectors, selected by the pattern control selector 420, and the order of their selection with the read and write macros in accordance with timing groups provided by element 425. In other words, the counter control 402, in conjunction with the timing groups 425, causes the pattern control selector 420 to function as a scheduler for the vectors and macros and counting therein into a complete test or burn-in sequence. Rather, as the counter control controls organization and selection order of the vectors, Applicants submit that the control counter does not form a control bit definition file configured to be added to the at least one vector. Therefore, Theodoseau does not contain each and every element of the claim, and does not anticipate the claimed invention.

Additionally, the Examiner asserts that Theodoseau discloses combining the macro, control bit, pattern formats, and global definition files to form a final vector to produce a final pattern. Applicants submit, however, that, assuming *arguendo* a macro definition file defining at least one vector is taught by Theodoseau's read macro or write macro, and the creation of a global definition file configured to alter the entire vector is taught by Theodoseau's refresh macro, which Applicants do not concede, Theodoseau does not disclose combing the macro, control bit, pattern formats, and global definition files to form a final vector to produce a final pattern. Instead, Theodoseau specifically discloses that a vector is developed "in accordance with the counter control 402 and *one of* read macro 406, write macro 404 or refresh macro 408 as may be selected by pattern control selector . . . ." (column 7, lines 10+; emphasis added). Thus, Applicants submit that the Examiner's interpretation of Theodoseau runs counter to the explicit disclosure of Theodoseau. Specifically, the Examiner asserts Theodoseau's use of

both a read or write macro, and a refresh macro. In contrast Theodoseau discloses the use of one of a read macro, write macro and refresh macro in developing a vector. Therefore, Theodoseau does not contain each and every element of the claim, and does not anticipate the claim.

Rejection of Dependent Claims 13 – 18 over Theodoseau

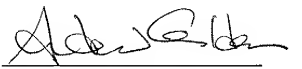
Applicants respectfully submit that claims 13 – 18 depend from a distinguishable independent claim, and are allowable based upon the allowability of the independent claim.

Accordingly, Applicants respectfully request that the rejection over claims 12 – 18 be withdrawn.

CONCLUSION

In view of the foregoing remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicants hereby make a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 09-0456.

Respectfully submitted,
Amy J. GOTTSCHE



Andrew M. Calderon
Reg. No. 38,093

November 17, 2006
GREENBLUM & BERNSTEIN, P.L.C.
1950 Roland Clarke Place
Reston, VA 20191
(703) 716-1191